Multi-Mode Primary Side Regulation QR-Buck CV/CC Controller

SA3540

Description

SA3540 is a high performance Primary Side Regulation (PSR) power switch with high precision CV/CC control ideal for charger applications. The IC can also support Quasi-Resonant (QR) Buck constant current topology for LED lighting if SEL pin is short to GND. In CV mode, SA3540 adopt Multi Mode Control which uses the hybrid of AM mode (Amplitude Modulation) and FM mode (Frequency Modulation) to improve system efficiency and reliability. In CC mode, the IC uses PFM control with line and load CC compensation. The IC can achieve audio noise free operation and optimized dynamic response. The built-in Cable Drop Compensation (CDC) function can provide excellent CV performance. SA3540 integrate functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), and VDD Clamping.

SA3540 is available in SOT23-6 package.

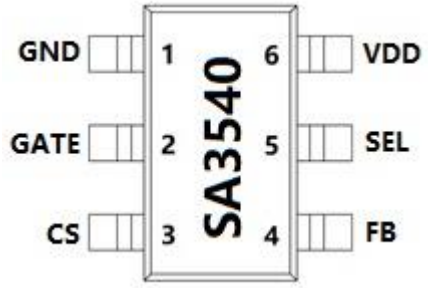
Features

- Support Flyback and Buck Topology:
  Flyback PSR Control (SEL= Floating)
  QR-Buck CC Control (SEL= GND)
- Multi Mode PSR Control
- Audio Noise Free Operation for PSR
- Optimized Dynamic Response for PSR
- Low Standby Power <70mW
- ±4% CC and CV Regulation
- Programmable Cable Drop Compensation:
  (CDC) in PSR CV Mode
- Built-in AC Line & Load CC Compensation
- Build in Protections:
  Short Load Protection (SLP)
  On-Chip Thermal Shutdown (OTP)
  Cycle-by-Cycle Current Limiting
  Leading Edge Blanking (LEB)
  Pin Floating Protection
- VDD OVP & Clamp

Applications

- Battery Chargers for Cellular Phones
- AC/DC Power Adapter
- LED Drives

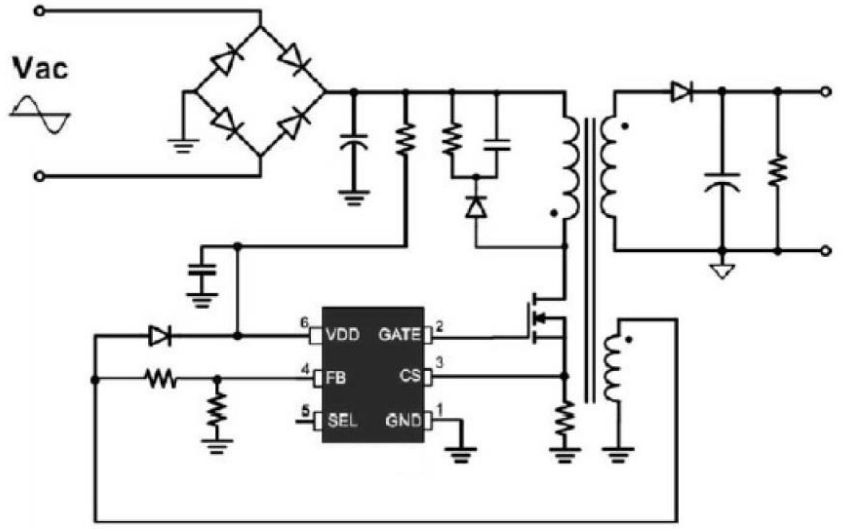
Pin Configuration

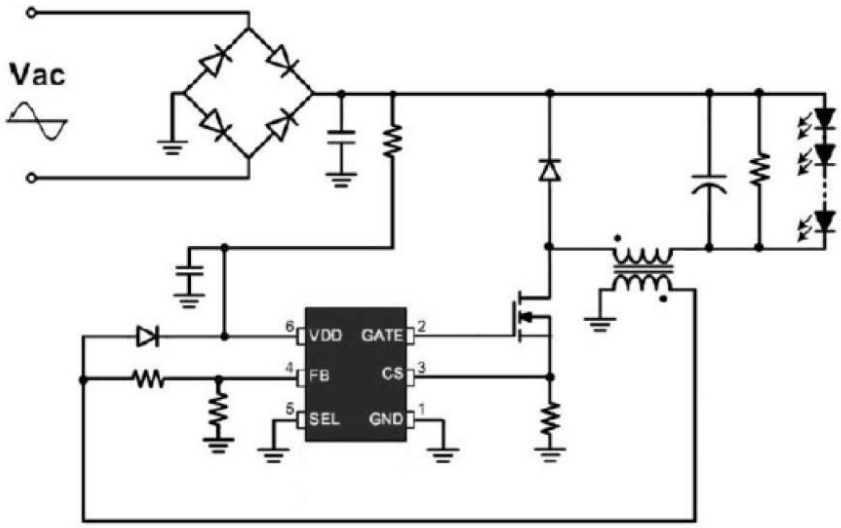


Pin Description

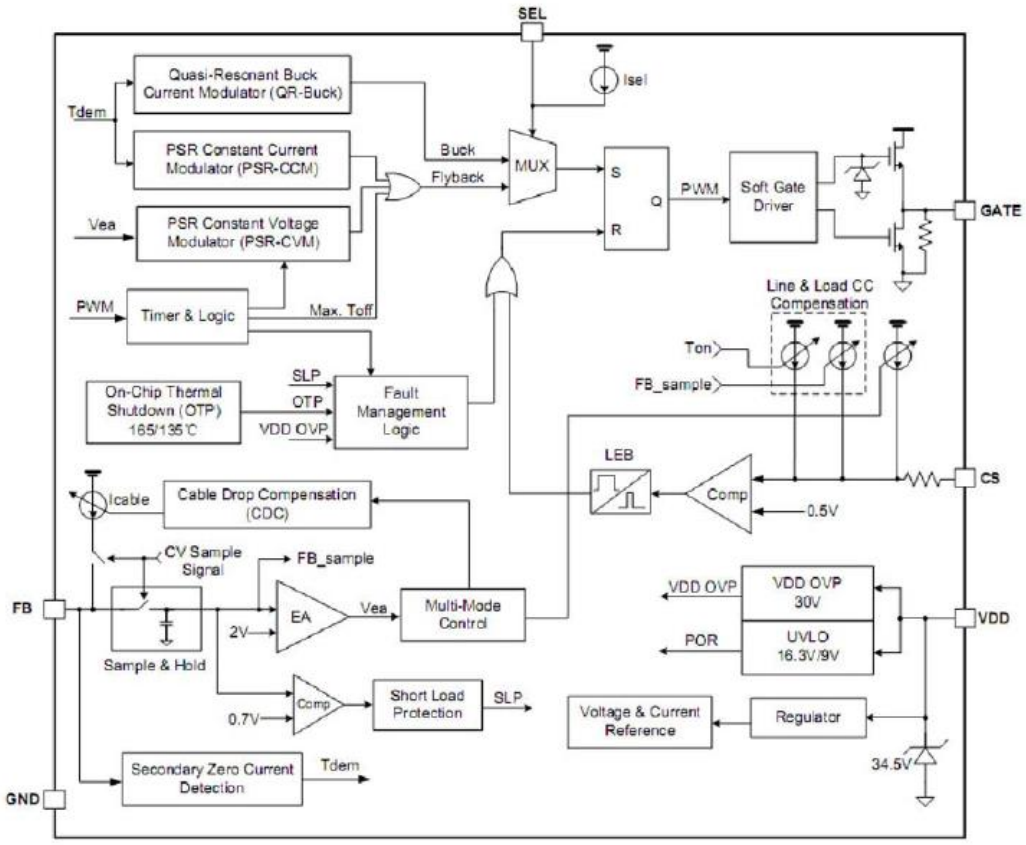
Pin	Name	Description
1	GND	The Ground of the IC
2	GATE	Gate Driver for External MOSFET Switch
3	CS	Current Sense Input Pin
4	FB	System feedback pin which regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of the auxiliary winding
5	SEL	Select Buck or Flyback configuration. Leave this pin floating for Flyback PSR control, while tying to GND for QR-Buck control
6	VDD	Power Supply Pin of the Chip

Typical Application





Functional Block Diagram



Absolute Maximum Ratings *1

Parameter Name	Value	Unit
VDD DC Supply Voltage	34.5	V
VDD DC Clamp Current	10	mA
GATE Pin	20	V
CS，SEL Voltage Range	-0.3 ~ 7	V
FB Voltage Range	-0.7 ~ 7	V
Package Thermal Resistance (SOP7)	85	℃/W
Maximum Junction Temperature	150	℃
Operating Temperature Range	-40 ~ +85	℃
Storage Temperature Range	-65 ~ +150	℃
Lead Temperature (Soldering, 10sec.)	260	℃
ESD Capability, HBM (Human Body Model)	3	KV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions *2

Parameter Name	Value	Unit
Supply Voltage, VDD	11 ~ 27	V
Operating Ambient Temperature	-40 ~ +85	℃
Maximum Switching Frequency @ Full Loading & Flyback PSR Mode	70	KHz
Minimum Switching Frequency @ Full Loading & Flyback PSR Mode	35	KHz

Electrical Characteristics

V_{DD} = 18V, T_A = 25°C, unless otherwise stated.

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage Section (VDD Pin)						
Start-up Current into VDD Pin	I_{VDD_ST}			2	20	μA
Operation Current	V_{DD_OP}	V_{FB}=3V		1.0	1.5	mA
Standby Current	$I_{VDD\_standby}$			0.5	1.0	mA
VDD Under Voltage Lockout Exit	V_{DD_ON}		15.0	16.3	17.5	V
VDD Under Voltage Lockout Enter	V_{DD_OFF}		8	9	10	V
VDD OVP Threshold	V_{DD_OVP}		28	30	32	V
VDD Zener Clamp Voltage	V_{DD_Clamp}	I_{VDD}=7mA	32.5	34.5	36.5	V
Flyback or Buck Selection Sections (FB Pin)						
Internal Error Amplifier(EA) Reference Input	V_{FB_REF}		1.97	2.00	2.03	V
Short Load Protection (SLP) Threshold	V_{FB_SLP}			0.7		V
Short Load Protection (SLP) Debounce Time	T_{FB_SHORT}			10		mS
Demagnetization Comparator Threshold	V_{FB_DEM}			25		mV
Minimum OFF time	T off min	*3		2		μS
Maximum OFF time	T off max	*3		5		mS
Maximum Cable Drop compensation current	I Cable_max			63		μA
Current Sense Input Section (CS Pin)						
CS Input Leading Edge Blanking Time	T_{LEB}			500		nS
Current Limiting Threshold	$V_{cs(max)}$		490	500	510	mV
Over Current Detection and Control Delay	T_{D_OCP}	GATE=0.5nF		100		nS
GATE Driver Section (GATE Pin) (Note 3)						
GATE Clamp Voltage	V_{G_Clamp}	VDD=24V				
OUTPUT Rising Time	T_ R	GATE=0.5nF				
OUTPUT Falling Time	T_ F	GATE=0.5nF				
Control Function Section (SEL Pin)						
SEL Pin Floating Voltage	$V_{SEL(floating)}$	*3		5.7		V
Internal SEL Pin Pull up Current	I_{SEL}	*3		35		μA

Over Temperature Protection						
Thermal Shutdown	T_{SD}	*3		165		℃
Thermal Recovery	T_{RC}	*3		135		℃

*1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

*2. The device is not guaranteed to function outside its operating conditions.

*3. Guaranteed by the Design

Application Summary

SA3540 is family of multi mode, highly integrated DCM (Discontinuous Conduction Mode) Primary Side Regulation (PSR) power switch. The built-in high precision CV/CC control with high level protection features makes it suitable for offline small power converter applications.

System Start-Up Operation

Before the IC starts to work, it consumes only startup current (typically 2μA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches UVLO turn-on voltage of 16.3V (typical), SA3540 begin switching and the IC operation current is increased to be 1mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage. Once SA3540 enter very low frequency FM (Frequency Modulation) mode, the operating current is reduced to be 0.5mA typically, which helps to reduce the standby power loss.

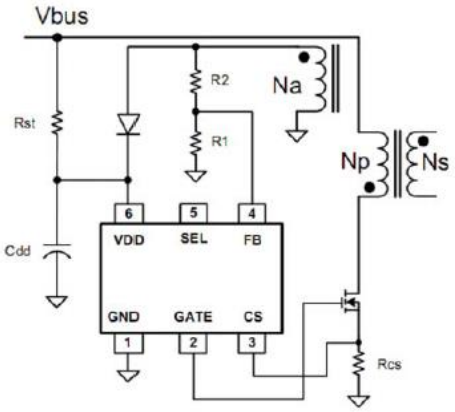


Fig.1

PSR Constant Voltage Modulation (PSR-CVM)

In primary side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. Fig.2 illustrates the CV sampling signal timing wave form in SA3540.

As shown in Fig.2, it is clear that there is a down slope representing a decreasing total rectifier Vf and its voltage drop as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the CV sampling signal blocks the leakage inductance reset and ringing. When the CV sampling process is over, the internal sample/hold (S&H) circuit captures the error signal and amplifies it through the internal Error Amplifier (EA). The output of EA is sent to the PSR Constant Voltage Modulator (PSR-CVM)

for CV control. The internal reference voltage for EA is trimmed to 2V with high accuracy.

During the CV sampling process, an internal variable current source is flowing to FB pin for Cable Drop Compensation (CDC). Thus, there is a step at FB pin in the transformer demagnetization process, as shown in Fig.2. Fig.2 also illustrates the equation for "demagnetization plateau", where Vo and VF is the output voltage and diode forward voltage; R1 and R2 is the resistor divider connected from the auxiliary winding to FB Pin, Ns and Na are secondary winding and auxiliary winding respectively. When system enters over load condition, the output voltage falls down and the FB sampled voltage should be lower than 2V internal reference which makes system enter CC Mode automatically.

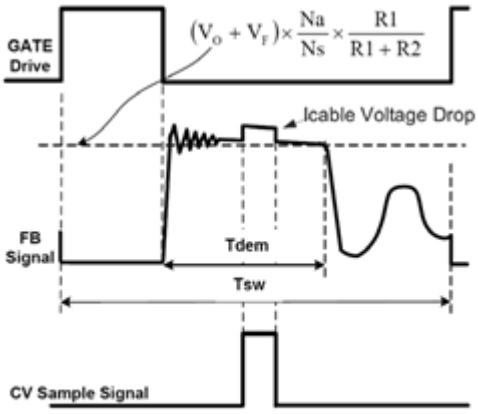


Fig.2

PSR Constant Current Modulation (PSR-CCM)

Timing information at the FB pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary peak current is at Ipp(max), as shown in Fig.3.

Referring to Fig.3 above, the primary peak current, transformer turns ratio, secondary demagnetization time (Tdem), and switching period (Tsw) determines the secondary average output current Iout. Ignoring leakage inductance effects, the equation for average output current is shown in Fig.3. When the average output current Iout reaches the regulation reference in the PSR Constant Current Modulator (PSR-CCM) block, the IC operates in pulse frequency modulation (PFM) mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold. In SA3540, the ratio between Tdem and Tsw in CC mode is 1/2. Therefore, the average output current can be expressed as:

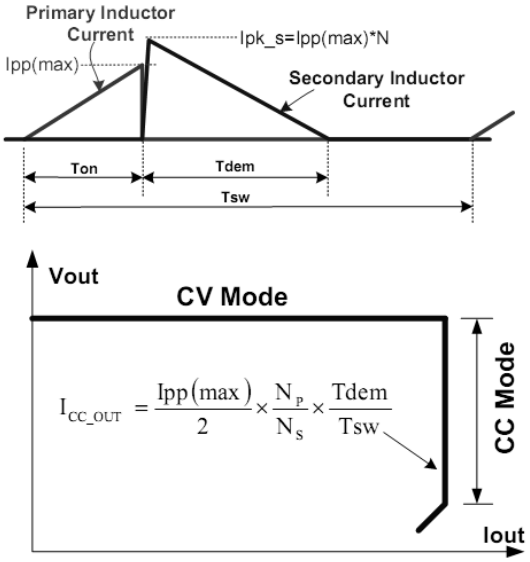


Fig.3

$$I_{PSR\_CC\_OUT}(mA) \cong \frac{1}{4} \times N \times \frac{500mV}{R_{CS}(\Omega)}$$

In the equation above,

N----The turn ratio of primary side winding to secondary side winding.

Rcs--- the sensing resistor connected between the power MOSFET source to GND.

Quasi Resonant Buck (QR-Buck) Constant Current Control for LED Lighting

If SEL pin is short to GND, SA3540 will works in Quasi-Resonant Buck mode. In QR-Buck mode,the IC keeps CS peak current constant and starts new PWM cycle with valley switching. Therefore, high precision CC and high conversion efficiency can be achieved simultaneously. The average output current is given by:

$$I_{Buck\_CC\_OUT}(mA) \cong \frac{1}{2} \times \frac{500mV}{Rcs(\Omega)}$$

Multi Mode Control in CV Mode

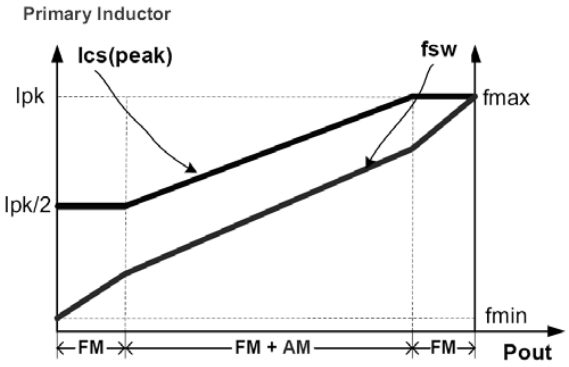


Fig.4

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude shown in the Fig 4. Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 70mW.

Programmable Cable Drop Compensation (CDC) in CV Mode

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In SA3540, an offset voltage is generated at FB pin by an internal current source (modulated by CDC block, as shown in Fig.5) flowing into the resistor divider. The current is proportional to the switching period, thus, it is inversely proportional to the output power Pout. Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. By adjusting the resistance of R1 and R2 (as shown in Fig5.), the cable loss compensation can be programmed. The percentage of maximum compensation is given by:

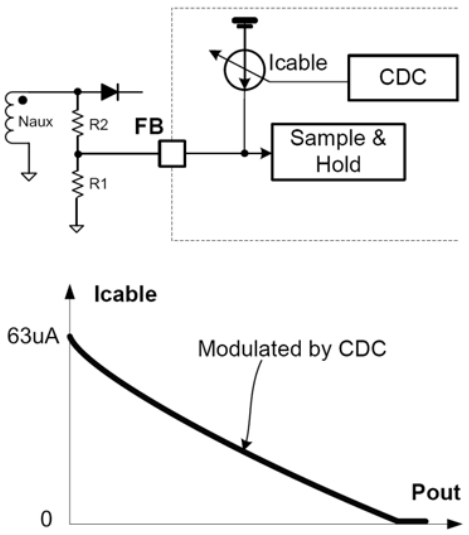


Fig.5

$$\frac{\Delta V(cable)}{Vout} \approx \frac{Icable\_\max \times (R1//R2)}{V_{FB\_REF}} \times 100\%$$

For example, R1=3KΩ , R2=18KΩ , The percentage of maximum compensation is given by:

$$\frac{\Delta V(cable)}{Vout} \approx \frac{63\mu A \times (3K//18K)}{V_{FB\_REF}} \times 100\% = 8.1\%$$

Optimized Dynamic Response for PSR

In SA3540, the dynamic response performance is optimized to meet USB charge requirements.

Audio Noise Free Operation for PSR

As mentioned above, the multi-mode CV control with a hybrid of FM and AM provides frequency modulation. An internal current source flowing to CS pin realizes CS peak voltage modulation. In SA3540, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

Short Load Protection (SLP)

In SA3540, the output is sampled on FB pin and then compared with a threshold of UVP (0.7V typically) after an internal blanking time (10ms typical). In SA3540, when sensed FB voltage is below 0.7V, the IC will enter into Short Load Protection (SLP)mode, in which the IC will enter into auto recovery protection mode.

VDD Over Voltage Protection (OVP) and Zener Clamp

When VDD voltage is higher than 30V (typical), the IC will stop switching. This will cause VDD fall down to be lower than VDD_OFF (typical 9V) and then the system will restart up again. An internal 34.5V (typical) Zener clamp is integrated to prevent the IC from damage.

On Chip Thermal Shutdown (OTP)

When the IC temperature is over 165 ℃, the IC shuts down. Only when the IC temperature drops to 135 ℃, IC will restart.

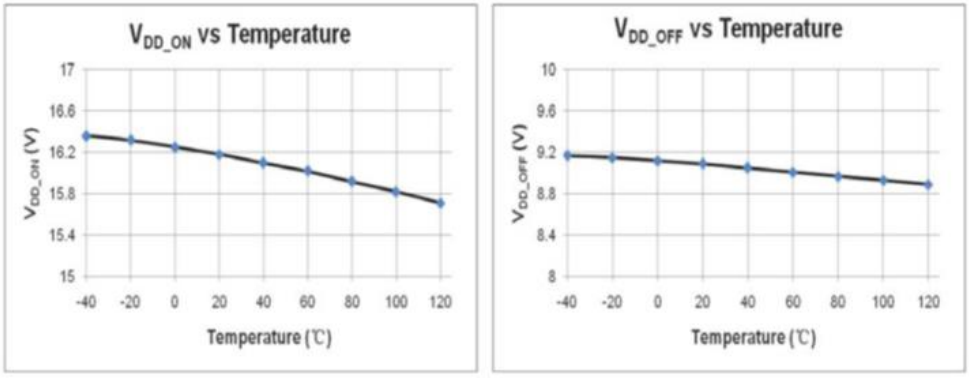
Pin Floating Protection

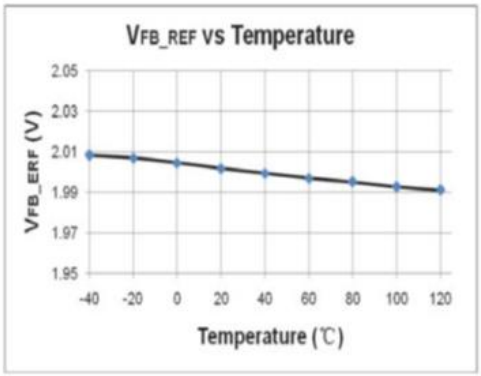
In SA3540, if pin floating situation occurs, the IC is designed to have no damage to system.

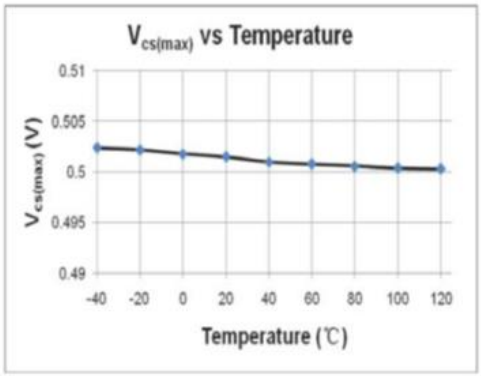
Soft Totem-Pole Gate Driver

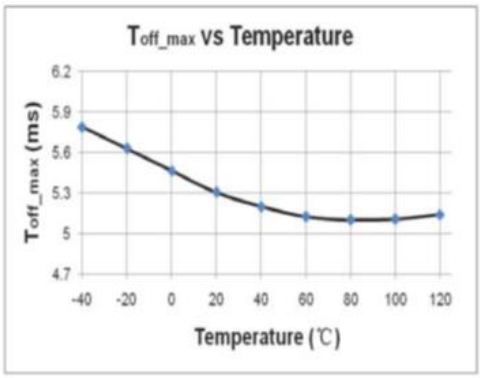
SA3540 have soft totem-pole gate driver with optimized EMI performance. An internal 16V clamp is added for power MOSFET gate protection when high VDD input.

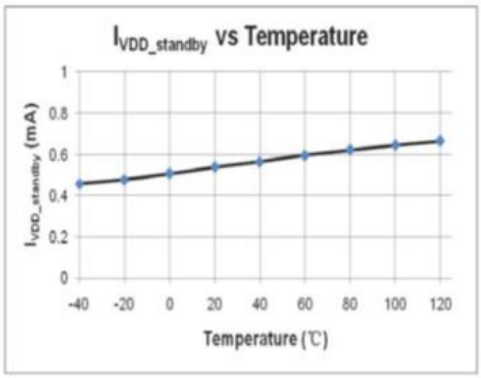
Characteristics Curve











Package outline

SOT23-6L **UNIT: mm**

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.45
A1	0	–	0.15
A2	0.90	1.10	1.30
A3	0.60	0.65	0.70
b	0.39	–	0.49
b1	0.38	0.40	0.45
c	0.12	–	0.19
c1	0.11	0.13	0.15
D	2.85	2.95	3.05
E	2.60	2.80	3.00
E1	1.55	1.65	1.75
e	0.85	0.95	1.05
e1	1.80	1.90	2.00
L	0.35	0.45	0.60
L1	0.59REF		
L2	0.25BSC		
R	0.05	–	–
R1	0.05	–	0.20
θ	0°	–	8°
θ1	8°	10°	12°
θ2	8°	10°	12°