Description

SA4876 is a high performance current mode PWM power switch for offline flyback converter applications. The IC has built-in General Primary Side CC control, which simplifies isolated power supply design that requires CC regulation of the output.

In SA4876, PWM switching frequency with shuffling is fixed to 65KHz and is trimmed to tight range. The IC has built-in green and burst mode control for light and zero loadings, which can achieve less than 75mW standby power .

SA4876 integrates functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), Over Load Protection (OLP), On-Chip Thermal Shutdown (OTP), Soft Start, VDD Clamping, etc.

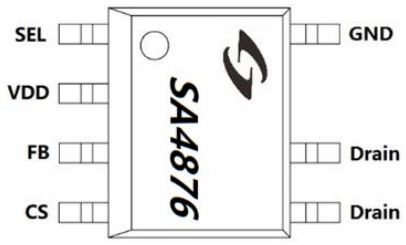
Features

- General Primary Side Constant-Current (CC) Control Supports DCM and CCM Operation
- ±5% CC Regulation , ±1% CV Regulation with Fast Dynamic Response
- CC Algorithm Compensates for Line Variation and Transformer Inductance Tolerance
- Less than 75mW Standby Power
- Current Mode Control
- Built-in Frequency Shuffling
- Fixed 65KHz Switching Frequency
- Green Mode and Burst Mode Control
- On-chip Thermal Shutdown
- Cycle-by-Cycle Current Limiting
- Built-in Leading Edge Blanking
- Built-in Slope Compensation
- Very Low Startup and Operation Current
- Available with SOP-7L Package

Applications

- Battery Chargers for Cellular Phones
- AC/DC Power Adapter
- Motor Driver Power Supply

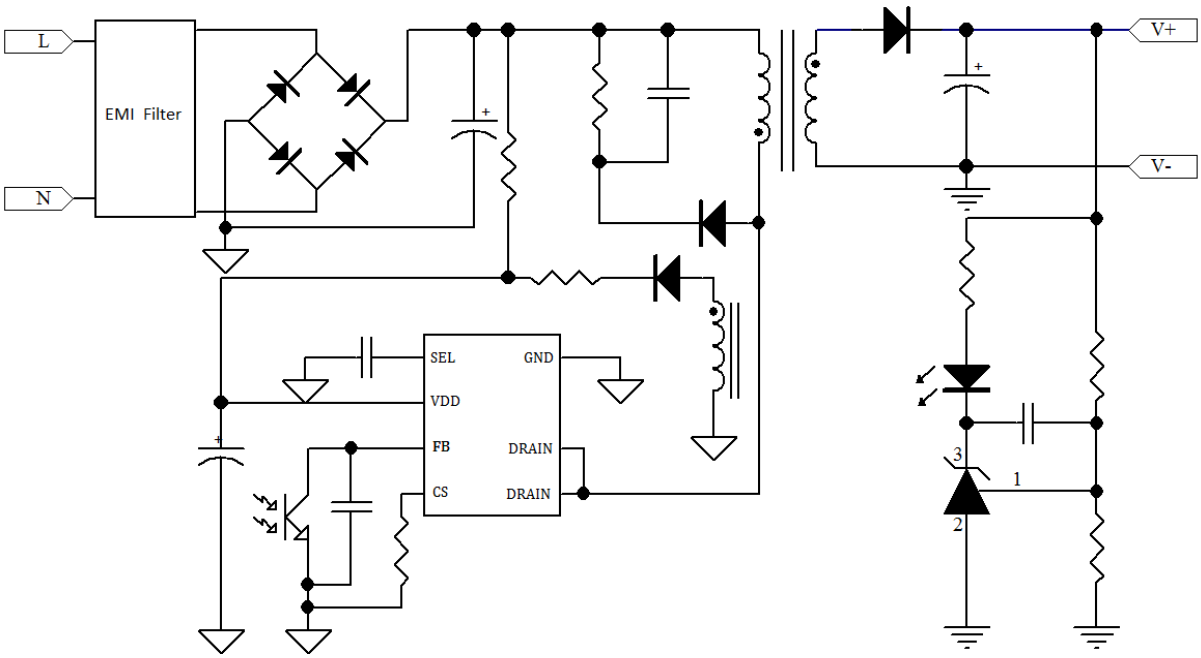
Pin Configuration



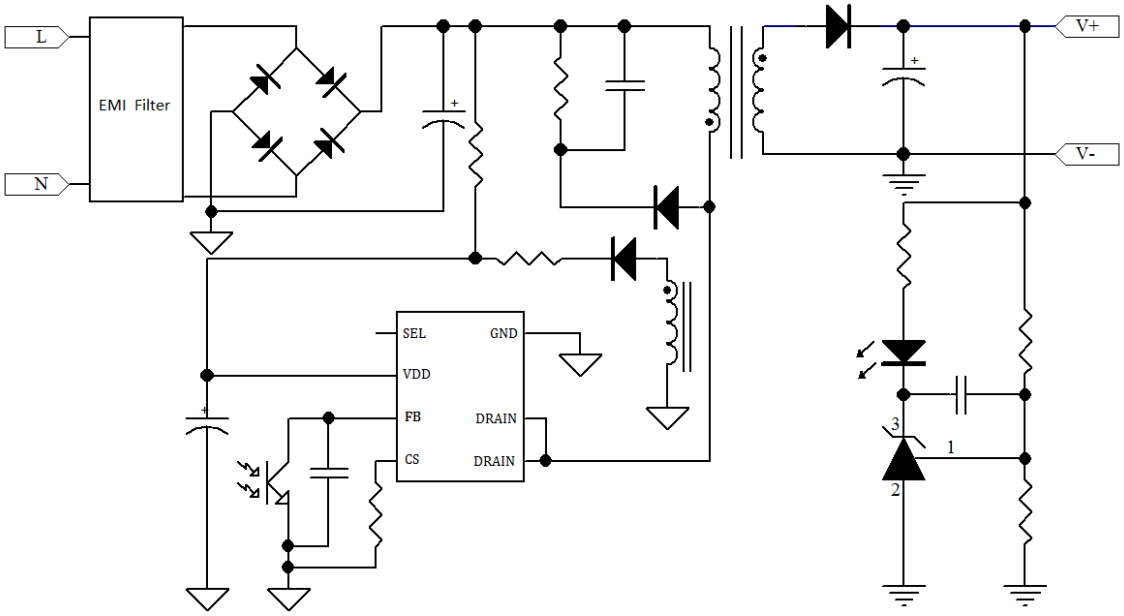
Pin Description

Pin	Name	Description
1	SEL	Connect a capacitor between SEL and GND, the IC will work in CC/CV mode. If SEL pin is floating, the IC will work in CV mode only.
2	VDD	IC Supply Voltage input
3	FB	Feedback input. The loop regulation is achieved by connecting a photocoupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 4.
4	CS	Current Sense Input Pin
5,6	GATE	The Power MOSFET Drain
7	GND	IC Ground

Typical Application

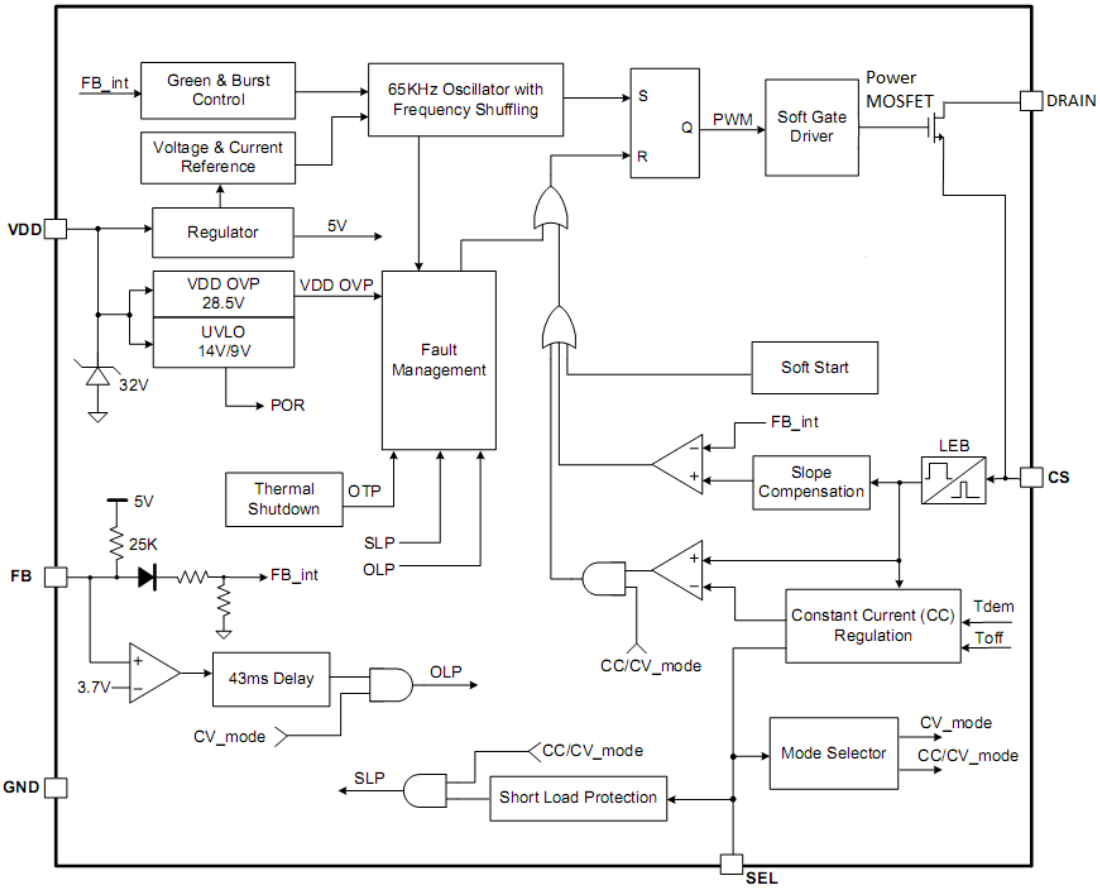


(For Applications with CC/CV Control)



(For Applications with Only CV Control)

Functional Block Diagram



Absolute Maximum Ratings *1

Parameter Name	Value	Unit
VDD DC Supply Voltage	30	V
VDD DC Clamp Current	10	mA
FB, CS, SEL Voltage Range	-0.3 ~ 7	V
DRAIN Voltage Range	-0.3 ~ 600	V
Package Thermal Resistance	165	℃/W
Maximum Junction Temperature	175	℃
Operating Temperature Range	-40 ~ +85	℃
Storage Temperature Range	-65 ~ +150	℃
Lead Temperature (Soldering, 10sec.)	260	℃
ESD Capability, HBM (Human Body Model)	4	KV
ESD Capability, MM (Machine Model)	500	V

Recommended Operation Conditions *2

Parameter Name	Value	Unit
Supply Voltage, VDD	10～26	V
Operating Ambient Temperature	-40 ~ +85	℃

Electrical Characteristics

V_{DD} = 20V, T_A = 25ºC, unless otherwise stated.

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage Section (VDD Pin)						
Start-up Current into VDD Pin	I_{VDD_ST}			2	20	μA
Operation Current	V_{DD_OP}	V_{FB}=3V, GATE=1nF		1.2	2	mA
Standby Current	$I_{VDD\_standby}$			0.6	1.0	mA
VDD Under Voltage Lockout Exit	V_{DD_ON}		19	21	22.5	V
VDD Under Voltage Lockout Enter	V_{DD_OFF}		8	9	10	V
VDD OVP Threshold	V_{DD_OVP}		29	31	33	V
VDD Zener Clamp Voltage	V_{DD_Clamp}	I_{VDD}=7mA	33	35	37	V
Flyback or Buck Selection Sections (FB Pin)						
FB Open Voltage	V_{FB_open}			5.5		V
FB Short Circuit Current	I_{FB_Short}	Short FB Pin to GND, Measure Current		0.3		mA
FB Input Impedance	Z_{FB_IN}			20		Kohm
PWM Gain	A_{CS}	$\Delta V_{FB}/\Delta V_{CS}$		2.0		V/V
FB Under Voltage GATE Clock is OFF	V_{SKIP}			1		V
Power Limiting FB Threshold Voltage	V_{TH_OLP}			3.6		V
Power Limiting Debounce Time	T_{D_OLP}	SEL Pin is floating		75		ms
Current Sense Input Section (CS Pin)						
CS Input Leading Edge Blanking Time	T_{LEB}			250		nS
Current Limiting Threshold	$V_{CS(MAX)}$		0.97	1.0	1.03	V
Over Current Detection and Control Delay	T_{D_OCP}	GATE=1nF		70		nS
Oscillator Section						
Normal Oscillation Frequency	F_{OSC}		60	65	70	KHz
Frequency Shuffling Range	$\Delta F_{(shuffle)}/F_{OSC}$		-4		4	%
Frequency Shuffling Period	$T_{(shuffle)}$			32		ms
Maximum Switching Duty Cycle	D_{MAX}			66.7		%
Burst Mode Base Frequency	F_{BURST}			22		KHz
CC Loop Regulation Section (SEL=Capacitor)						
Internal Reference for CC Loop Regulation	$V_{CC\_REG\_SEL}$	SEL Pin=Capacitor	194	200	206	mV
Internal Source Current for CC Loop Regulation	$I_{CC\_SEL\_SOURCE}$	SEL Pin=Capacitor		20		uA

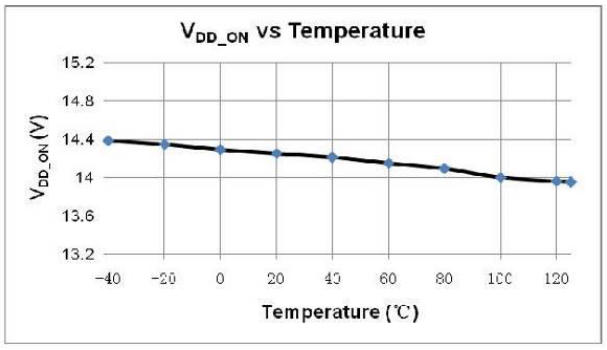
Short Load Protection (SLP) Threshold	$V_{CC\_SLP\_SEL}$	SEL Pin=Capacitor		0.7		V
Short Load Protection (SLP) Debounce Time	$T_{CC\_SHORT\_SEL}$	SEL Pin=Capacitor		43		ms
On-Chip Thermal Shutdown						
Thermal Shutdown	T_{SD}	*3		165		℃
Thermal Recovery	T_{RC}	*3		140		℃
Power MOSFET Section (SA4876S) *3						
Power MOSFET Drain Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	600			V
Static Drain-Source On Resistance	R_{DSON}	V_{GS}=10V, I_D=1A		1.8		Ω
Power MOSFET Section (SA4876V) *3						
Power MOSFET Drain Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	600			V
Static Drain-Source On Resistance	R_{DSON}	V_{GS}=10V, I_D=1A		2.2		Ω
Power MOSFET Section (SA4876HV) *3						
Power MOSFET Drain Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	650			V
Static Drain-Source On Resistance	R_{DSON}	V_{GS}=10V, I_D=1A		2.6		Ω

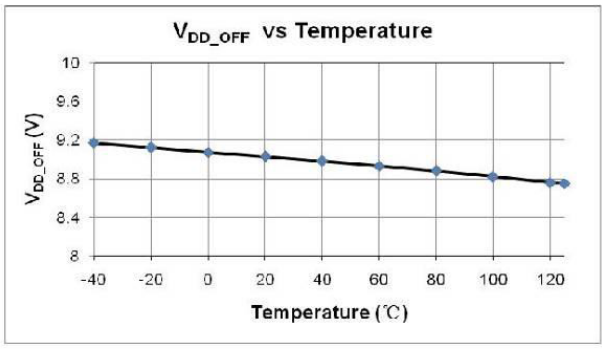
*1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

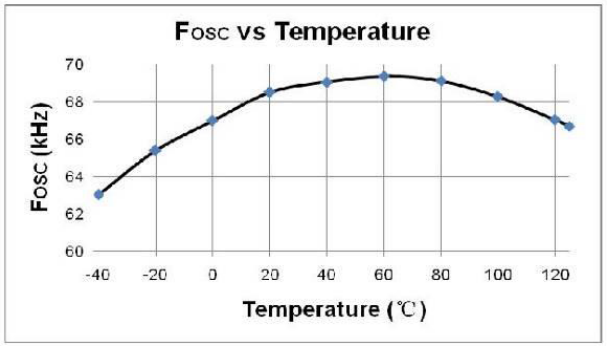
*2. The device is not guaranteed to function outside its operating conditions.

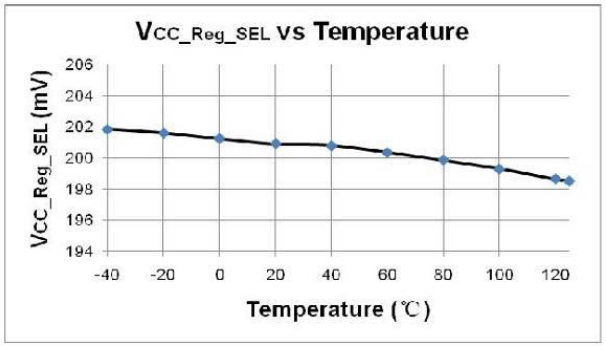
*3. Guaranteed by the Design

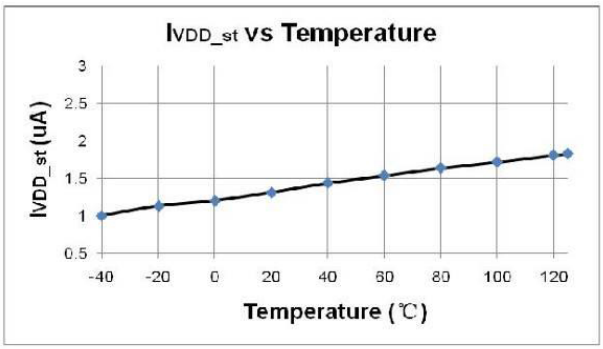
Characterization Plots

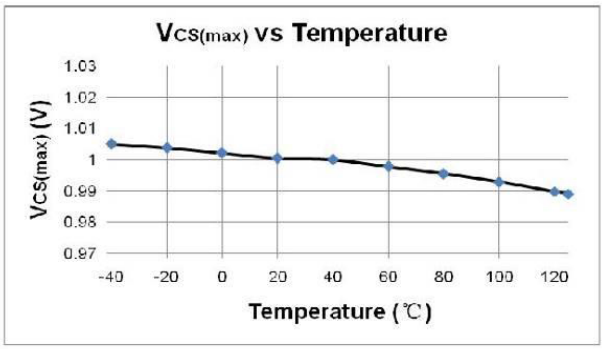


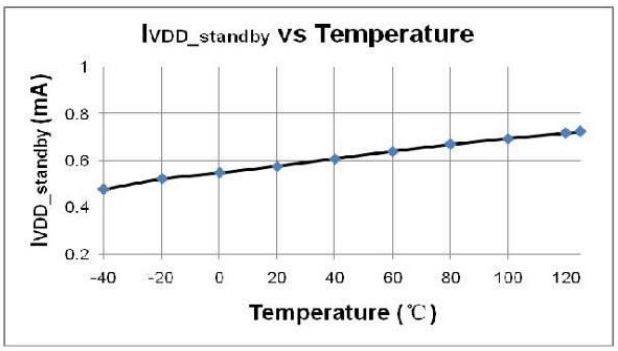












Peration Description

SA4876 is a high performance current mode PWM controller for offline flyback charger, motor driver power supply, and adapter applications. The IC has built-in General Primary Side CC control, which simplifies isolated power supply design that requires CC regulation of the output.

System Start-Up Operation and IC Operation Current

Before the IC starts to work, it consumes only startup current (typically 2uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches V_{DD_ON} (typical 21V), SA4876 begins switching and the IC operation current is increased to be 1.2mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage. When the IC enters into burst mode, the IC operation current will decrease further, thus less than 75mW standby power.

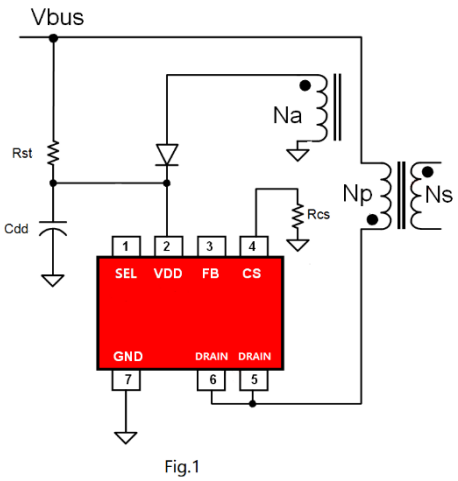


Fig.1

General Primary Side Constant Current Modulation for DCM/CCM

Compared to conventional flyback DCM Primary Side Regulation (PSR) Constant Current (CC) method, a General Primary Side Constant Current Modulation algorithm is adopted in SA4876

which supports transformer DCM and CCM operation simultaneously.

Fig.2 illustrates the key waveform of a flyback converter operating in DCM and CCM, respectively. The output current I_{out} of each mode is estimated by calculating the average current of secondary or primary inductor over one switching cycle:

$$I_{OUT} = \frac{\int_0^{T_S} I_S(t)dt}{T_S} = N \times \frac{\int_0^{T_S} I_P(t)dt}{T_S} \quad (1)$$

In Eq.(1) above, $I_{s(t)}$ is the secondary inductor or rectification diode current inductor current, N is primary-to-secondary transformer turn ratio.

The average secondary inductor current in both DCM and CCM can be expressed in a same form, as a product of secondary inductor discharge time T_{DIS} and secondary inductor current at the middle of T_{DIS}, such as:

$$\int_0^{T_S} I_S(t)dt = I_{mid\_S} \times T_{DIS} = N \times I_{mid\_P} \times T_{DIS} \quad (2)$$

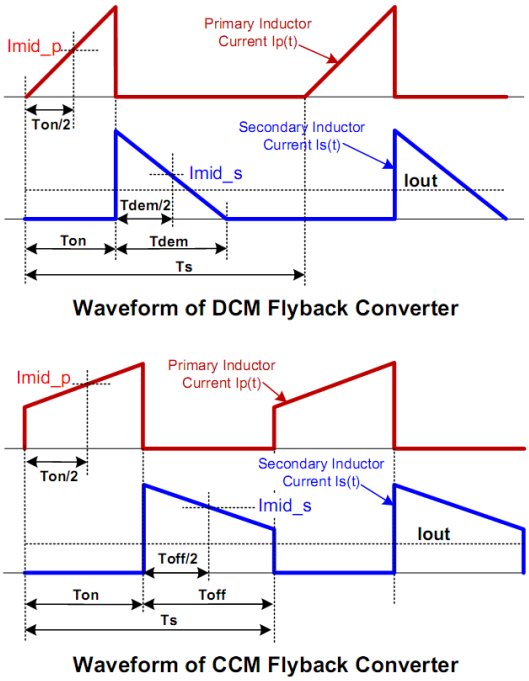


Fig.2

In Eq.(2), I_{mid_S} and I_{mid_P} are the secondary and primary inductor current at the middle of T_{DIS} and T_{ON} respectively, as shown in Fig.2. T_{DIS} can be given by the following equation:

$$T_{DIS} = \begin{cases} T_{DEM} & (\text{for DCM mode}) \\ T_{OFF} & (\text{for CCM mode}) \end{cases} \quad (3)$$

In Eq.(3), $T_{DIS}=T_{DEM}$ for DCM operation and $T_{DIS}=T_{OFF}$ for CCM operation respectively.

Combined with Eq.(1) to Eq. (3), the average output current I_{out} can be expressed as:

$$I_{OUT} = N \times I_{mid\_P} \times \frac{T_{DIS}}{T_S} = N \times \frac{V_{mid\_P}}{R_{CS}} \times \frac{T_{DIS}}{T_S} \quad (4)$$

In Eq.(4), R_{CS} is the sensing resistor connected between the power MOSFET source to GND. V_{mid_P} is sampled R_{CS} voltage at the middle of primary power MOSFET conduction time.

In SA4876, the product of V_{mid_P} and T_{DIS} is kept constant by the IC's internal PWM CC regulation loop. The switching frequency is trimmed to 65KHz in SA4876.Therefore, the average output current I_{out} will be well regulated and given by:

$$I_{CC\_OUT}(mA) = N \times \frac{V_{CC\_Reg}}{Rcs} \cong N \times \frac{200mV}{Rcs(\Omega)} \quad (5)$$

Demagnetization Detection without Auxiliary Winding

In SA4876, the transformer core demagnetization is detected by monitoring the coupling current flowing through the parasitic capacitor C_{rss} between the drain and gate of power MOSFET. When the transformer is fully demagnetized, the drain voltage evolution is governed by the

resonating energy transfer between the transformer inductor and the parasitic capacitance of the drain. These voltage oscillations create current oscillation in the parasitic capacitor C_{rss}. A negative current takes place during the decreasing part of the drain oscillation, and a positive current during the increasing part. The transformer demagnetization time corresponds to the inversion of the current by detecting this point, as shown in Fig.3

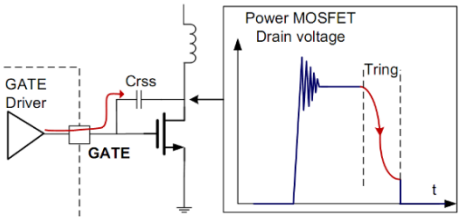


Fig.3

Mode Selection for CV and CC/CV

The load of SEL pin determines the operation mode of IC. In SA4876, the IC will work in CC/CV mode if an external capacitor is connected between SEL pin and GND. Otherwise, if SEL pin is floating, the IC will work in only CV mode.

±5% CC Regulation, ±1% CV Regulation with Fast Dynamic Response

The CC algorithm in SA4876 compensates line variation and transformer inductance tolerance. The IC can achieve ±5% CC regulation. The IC can also achieve ±1% CV regulation and fast dynamic response, due to the same control method as convention PWM controllers.

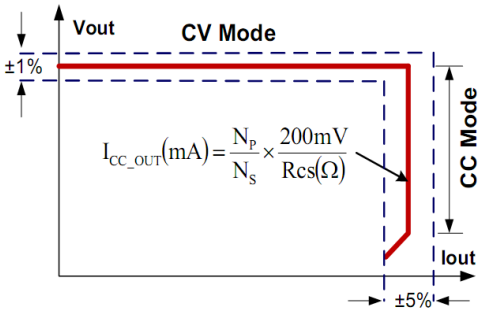


Fig.4

Oscillator with Frequency Shuffling

PWM switching frequency in SA4876 is fixed to 65KHz and is trimmed to tight range. To improve system EMI performance, SA4876 operates the system with 4% frequency shuffling around setting frequency.

Built-in Slope Compensation

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in higher than 50% of the duty-cycle. In SA4876 the slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the PWM comparator is disabled and cannot switch off the gate driver.

Green Mode Operation

Since the main power dissipation at light/zero load in a switching mode power supply is from

the switching loss which is proportional to the PWM switching frequency. To meet green mode requirement, it is necessary to reduce the switching cycles under such conditions either by skipping some switching pulses or by reducing the switching frequency.

Smooth Frequency Foldback

In SA4876, a Proprietary "Smooth Frequency Foldback" function is integrated to foldback the PWM switching frequency when the loading is light. Compared to the other frequency reduction implementations, this technique can reduce the PWM frequency smoothly without audible noise.

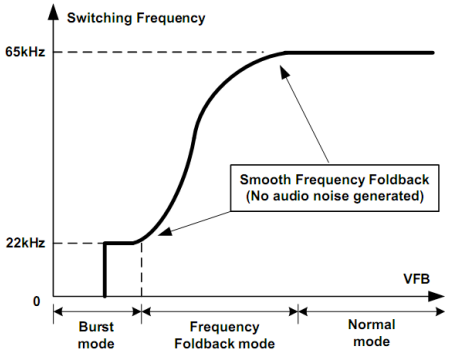


Fig.5

Burst Mode Control

When the loading is very small, the system enters into burst mode. When VFB drops below V_{skip}, SA4876 will stop switching and output voltage starts to drop (as shown in Fig.6), which causes the V_{FB} to rise. Once V_{FB} rises above V_{skip}, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

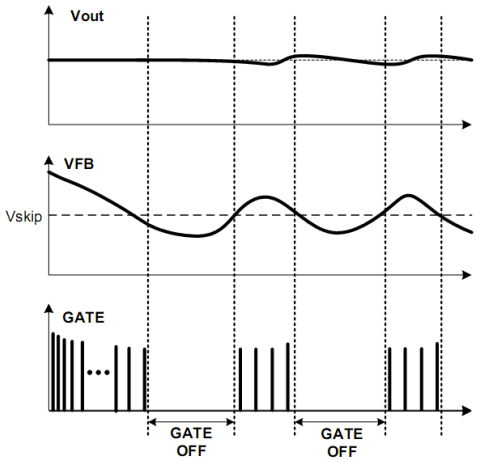


Fig.6

On Chip Thermal Shutdown (OTP)

When the IC temperature is over 165℃ , the IC shuts down. Only when the IC temperature drops to 140℃, IC will restart.

Soft Start

SA4876 features an internal 20ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

Constant Power Limiting in CV Mode

In CV mode, a proprietary "Constant Power Limiting" block is integrated to achieve constant maximum output power capability over universal AC input range. Based on the duty cycle information, the IC generates OCP threshold according to a proprietary analog algorithm.

Short Load Protection (SLP) in CC/CV Mode

In SA4876, if the IC works in CC/CV mode and CC voltage is below 0.7V, the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode.

Over Load Protection (OLP) in CV Mode

In CV mode and if over load occurs, a fault is detected. If this fault is present for more than 75ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode

protection as mentioned above. The 43ms delay time is to prevent the false trigger from the power-on and turn-off transient.

VDD Over Voltage Protection (OVP) and Zener Clamp

When V_{DD} voltage is higher than 31V (typical), the IC will stop switching. This will cause V_{DD} fall down to be lower than V_{DD_OFF} (typical 9V) and then the system will restart up again. An internal 35V (typical) zener clamp is integrated to prevent the IC from damage.

Auto Recovery Mode Protection

As shown in Fig.7, once a fault condition is detected, PWM switching will stop. This will cause V_{DD} to fall because no power is delivered form the auxiliary winding. When V_{DD} falls to V_{DD_OFF} (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes V_{DD} to rise. The system begins switching when V_{DD} reaches to V_{DD_ON} (typical 14V). However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

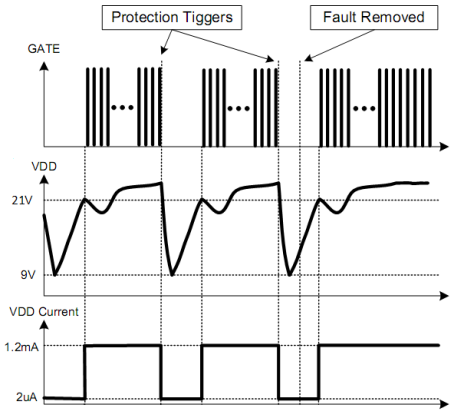


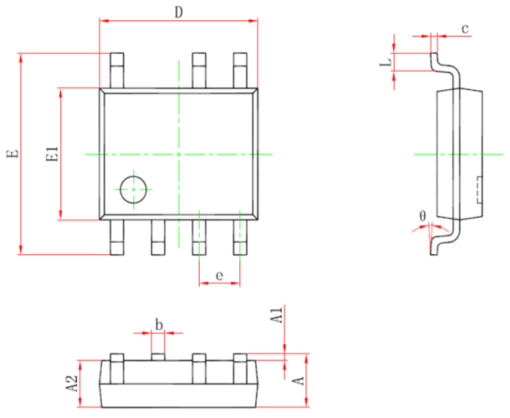
Fig.7

Soft Gate Driver

The output stage of SA4876 is a totem-pole gate driver with optimized EMI performance. An internal gate clamp is added for MOSFET gate protection at higher than expected VDD input.

Package Dimensions

SOP-7L UNIT: mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°